Synthesis Report :

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# Vivado v2018.3 (64-bit)

# SW Build 2405991 on Thu Dec 6 23:38:27 MST 2018

# IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

# Start of session at: Sun Apr 21 23:19:10 2019

# Process ID: 17828

# Current directory: C:/Users/TANUMON ROY/Desktop/DSD project/FIFO01/FIFO01.runs/synth\_1

# Command line: vivado.exe -log FIFO\_mem.vds -product Vivado -mode batch -messageDb vivado.pb -notrace -source FIFO\_mem.tcl

# Log file: C:/Users/TANUMON ROY/Desktop/DSD project/FIFO01/FIFO01.runs/synth\_1/FIFO\_mem.vds

# Journal file: C:/Users/TANUMON ROY/Desktop/DSD project/FIFO01/FIFO01.runs/synth\_1\vivado.jou

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source FIFO\_mem.tcl -notrace

create\_project: Time (s): cpu = 00:00:03 ; elapsed = 00:00:08 . Memory (MB): peak = 320.766 ; gain = 57.625

Command: synth\_design -top FIFO\_mem -part xc7z020clg484-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7z020'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 9212

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Starting Synthesize : Time (s): cpu = 00:00:05 ; elapsed = 00:00:07 . Memory (MB): peak = 431.059 ; gain = 97.719

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INFO: [Synth 8-6157] synthesizing module 'FIFO\_mem' [C:/Users/TANUMON ROY/Desktop/DSD project/FIFO01/FIFO01.srcs/sources\_1/new/FIFO\_mem.v:23]

Parameter DEPTH bound to: 3 - type: integer

Parameter MAX\_COUNT bound to: 3'b111

INFO: [Synth 8-226] default block is never used [C:/Users/TANUMON ROY/Desktop/DSD project/FIFO01/FIFO01.srcs/sources\_1/new/FIFO\_mem.v:88]

INFO: [Synth 8-6155] done synthesizing module 'FIFO\_mem' (1#1) [C:/Users/TANUMON ROY/Desktop/DSD project/FIFO01/FIFO01.srcs/sources\_1/new/FIFO\_mem.v:23]

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Finished Synthesize : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 487.484 ; gain = 154.145

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Finished Constraint Validation : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 487.484 ; gain = 154.145

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Start Loading Part and Timing Information

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Loading part: xc7z020clg484-1

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INFO: [Device 21-403] Loading part xc7z020clg484-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 487.484 ; gain = 154.145

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INFO: [Synth 8-5544] ROM "empty" won't be mapped to Block RAM because address size (3) smaller than threshold (5)

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:10 . Memory (MB): peak = 487.484 ; gain = 154.145

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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No constraint files found.

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

2 Input 3 Bit Adders := 4

+---Registers :

16 Bit Registers := 1

3 Bit Registers := 1

1 Bit Registers := 1

+---RAMs :

128 Bit RAMs := 1

+---Muxes :

2 Input 16 Bit Muxes := 2

4 Input 3 Bit Muxes := 1

4 Input 1 Bit Muxes := 1

2 Input 1 Bit Muxes := 3

3 Input 1 Bit Muxes := 1

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Finished RTL Component Statistics

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Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module FIFO\_mem

Detailed RTL Component Info :

+---Adders :

2 Input 3 Bit Adders := 4

+---Registers :

16 Bit Registers := 1

3 Bit Registers := 1

1 Bit Registers := 1

+---RAMs :

128 Bit RAMs := 1

+---Muxes :

2 Input 16 Bit Muxes := 2

4 Input 3 Bit Muxes := 1

4 Input 1 Bit Muxes := 1

2 Input 1 Bit Muxes := 3

3 Input 1 Bit Muxes := 1

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Finished RTL Hierarchical Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 220 (col length:60)

BRAMs: 280 (col length: RAMB18 60 RAMB36 30)

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Finished Part Resource Summary

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No constraint files found.

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

INFO: [Synth 8-5544] ROM "empty" won't be mapped to Block RAM because address size (3) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "full0" won't be mapped to Block RAM because address size (3) smaller than threshold (5)

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:14 ; elapsed = 00:00:22 . Memory (MB): peak = 639.918 ; gain = 306.578

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Start ROM, RAM, DSP and Shift Register Reporting

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Distributed RAM: Preliminary Mapping Report (see note below)

+------------+------------+-----------+----------------------+--------------+

|Module Name | RTL Object | Inference | Size (Depth x Width) | Primitives |

+------------+------------+-----------+----------------------+--------------+

|FIFO\_mem | fifo\_reg | Implied | 8 x 16 | RAM32M x 3 |

+------------+------------+-----------+----------------------+--------------+

Note: The table above is a preliminary report that shows the Distributed RAMs at the current stage of the synthesis flow. Some Distributed RAMs may be reimplemented as non Distributed RAM primitives later in the synthesis flow. Multiple instantiated RAMs are reported only once.

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Finished ROM, RAM, DSP and Shift Register Reporting

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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No constraint files found.

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:14 ; elapsed = 00:00:22 . Memory (MB): peak = 639.918 ; gain = 306.578

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Start ROM, RAM, DSP and Shift Register Reporting

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Distributed RAM: Final Mapping Report

+------------+------------+-----------+----------------------+--------------+

|Module Name | RTL Object | Inference | Size (Depth x Width) | Primitives |

+------------+------------+-----------+----------------------+--------------+

|FIFO\_mem | fifo\_reg | Implied | 8 x 16 | RAM32M x 3 |

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Finished ROM, RAM, DSP and Shift Register Reporting

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:14 ; elapsed = 00:00:22 . Memory (MB): peak = 649.445 ; gain = 316.105

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:16 ; elapsed = 00:00:25 . Memory (MB): peak = 649.445 ; gain = 316.105

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Report Check Netlist:

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| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:16 ; elapsed = 00:00:25 . Memory (MB): peak = 649.445 ; gain = 316.105

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:16 ; elapsed = 00:00:25 . Memory (MB): peak = 649.445 ; gain = 316.105

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:16 ; elapsed = 00:00:25 . Memory (MB): peak = 649.445 ; gain = 316.105

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:16 ; elapsed = 00:00:25 . Memory (MB): peak = 649.445 ; gain = 316.105

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:16 ; elapsed = 00:00:25 . Memory (MB): peak = 649.445 ; gain = 316.105

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Start Writing Synthesis Report

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Report BlackBoxes:

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| |BlackBox name |Instances |

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Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |BUFG | 1|

|2 |LUT1 | 1|

|3 |LUT3 | 2|

|4 |LUT4 | 5|

|5 |LUT5 | 19|

|6 |LUT6 | 6|

|7 |RAM32M | 3|

|8 |FDRE | 26|

|9 |IBUF | 20|

|10 |OBUF | 18|

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Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 101|

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:16 ; elapsed = 00:00:25 . Memory (MB): peak = 649.445 ; gain = 316.105

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:16 ; elapsed = 00:00:25 . Memory (MB): peak = 649.445 ; gain = 316.105

Synthesis Optimization Complete : Time (s): cpu = 00:00:16 ; elapsed = 00:00:25 . Memory (MB): peak = 649.445 ; gain = 316.105

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 3 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 1 inverter(s) to 3 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 756.000 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

A total of 3 instances were transformed.

RAM32M => RAM32M (inverted pins: WCLK) (RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32): 3 instances

INFO: [Common 17-83] Releasing license: Synthesis

15 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:26 ; elapsed = 00:00:49 . Memory (MB): peak = 756.000 ; gain = 435.234

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 756.000 ; gain = 0.000

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used\_in flags are set such that the constraints are ignored. This later case is used when running synth\_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

INFO: [Common 17-1381] The checkpoint 'C:/Users/TANUMON ROY/Desktop/DSD project/FIFO01/FIFO01.runs/synth\_1/FIFO\_mem.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file FIFO\_mem\_utilization\_synth.rpt -pb FIFO\_mem\_utilization\_synth.pb

INFO: [Common 17-206] Exiting Vivado at Sun Apr 21 23:20:29 2019...